Towards Automation Of 180nm, 90nm And 45nm Standard Cell Library Characterization

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Abstract

The focus of this paper is to study the parameters involved in the standard cell library characterization taking into account the three technologies nodes i.e., 180nm, 90nm & 45 nm. Commercial library cells are proprietary information of EDA companies. The companies usually impose certain restrictions on the access of these library cells. For example, Synopsys is offering Liberty NCX, Cadence has Virtuoso Foundation IP Characterization and MentorGraphics & Z-circuit technology (acquired by MentorGrapics) is offering Kronos for Standard Cell Library Characterization. Producing designs based on sub-micron technologies at a competitive cost has always been a challenge for manufacturers.

I. INTRODUCTION

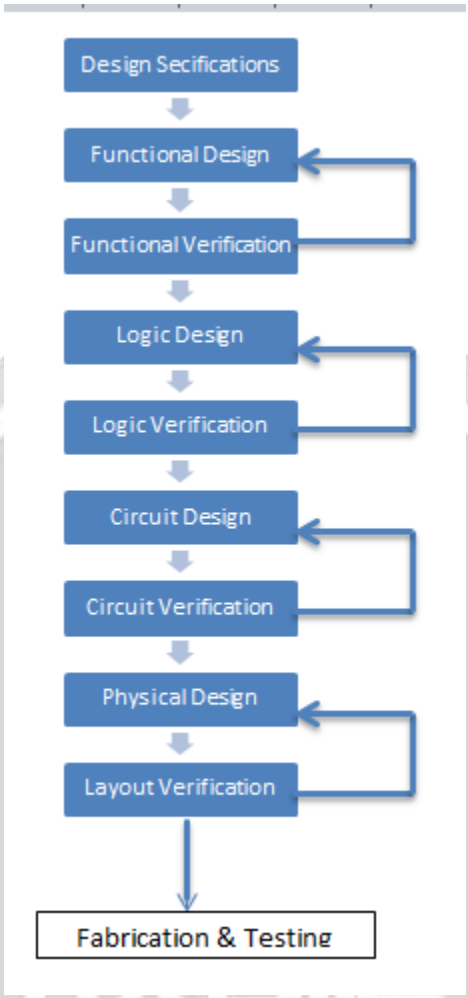
Standard cell library is a collection of combinational and sequential logic gates. It is an abstraction of specific logic gates, providing characteristics and description of these gates including area, timing and power. Standard cell methodology allows designer to focus on higher level circuit and system design without worrying too much about the detailed implementation of a specific cell.

The intent of the work is to create standard cell libraries at 180nm, 90nm & 45nm technology nodes along with the characterization results for academic and research purposes. The study of the involved parameters at different process(TT, FF, SS, FS, SF), temperature and voltage corners will be the part of the proposed work.

Cell Library Characterizarion is a process of analyzing a circuit using static and dynamic methods to generate models suitable for chip implementation. Standard Cell Library Characterization is basically done to analyze the logic cells in terms of area, performance and power. Along with this, implementation and fixing of the standard set of rules as per the specifications provided by the foundry. The key factor for the rapid growth of the integrated system is the use of ASIC (Application Specific Integrated Circuit) library for various system functions. It consists of well designed and verified blocks that shortens development time and manages complexity of the chip. The economic and efficient accomplishment of the ASIC designs depends on the choice of library. Therefore it is necessary to build the library that fulfills the design requirement.The main focus is to minimize the area of each standard cell. This will further cater the placement and routing of the logic blocks placed over integrated circuit in terms of reduction of the area of the whole chip with minimum change in the performance. So, the main focus is to design standard cells of Inverter, NOR, NAND, MUX, D-FlipFlop(Sequential Circuit) and Full Adder.

II. DIGITAL DESIGN FLOW

The project is concerned towards designing of standard cells. Digital Design Flow is described below:



The design flow starts from the specifications gained by the user/clients. As per the specification like technology node, Chip density, Area, Power, Timing etc, process of designing the standard cells started. The flow is then divided into 6 modules:

1. Starting from schematic design, creating symbol of the schematic will end up to the pre-layout simulations or schematic simulations.
2. Designing of the cell specific layout as per the standard Design Rule Checks (DRC). Followed by SPICE netlist extraction of the layout.
3. The next step will be to run Layout vs Schematic (LVS) check to validate the design.
4. Then post layout simulation will take place .
5. Parasitic Extraction then will be performed to analyze the design parasitics and the effects of the parasitics (resistance & capacitance) over the performance of the design.
6. After this, placement and route will come into picture.

Then we will follow all the above mentioned steps at different PVT corners by model selection and specification. Lastly the verification of the design will take place at these PVT corners.
To design a Standard Cells Library Characterization the following tools of Cadence Design Tool will be used:

TOOL	PURPOSE
Virtuoso Schematic Editor	Schematic Design
Spectre	Schematic Simulator
Virtuoso Layout Editor L	Layout Design
Calibre	Layout Verification (DRC,LVS)
Layout XL	Layout Simulation
Assura	Run DRC, LVS
RedHat (OS)	Environment

Input Files : .lib, .db, .def, .lef

.LIB(Liberty Timing File) : .lib is basically a timing model contains cell delays, transition, setup and hold time requirements. The design needs to be tested for PVT (Process Voltage and Temperature) corners. But for every PVT corner, the timing of the cells are different. Hence, there is .lib for every PVT corner.

.DB(Database file) : .db file is the technology library file. Like gdpk180nm, gdpk90nm etc.

.DEF(Design Exchange Format) : The DEF file basically contains the placement information of macros , standard cells, I/O pins and other physical entities. DEF generated by PnR are used by STAR RC extraction.

.LEF(Library Exchange Format) : The LEF file is the abstract view of cells. It only gives the idea about PR boundary, pin position and metal layer information of a cell.

III. REVIEW

Down scaling of the technology node may not have impact on the functional and behavioral aspects of the design but timing and performance are affected significantly. Starting from this the first study which we will be discussing is **"Characterizing VLSI Standard Cell Library".** This study has described a system for characterizing standard cell library, consisting of a stimuli database describing the characterizations requirements of each cell. Entire characterization system, called *ch,* using standard UNIX facilities like ***sh, awk, ed, sed, cpp*** etc. Geometrical circuit data is extracted from the GDSII description using **DRACULA** layout parasitic extractor.

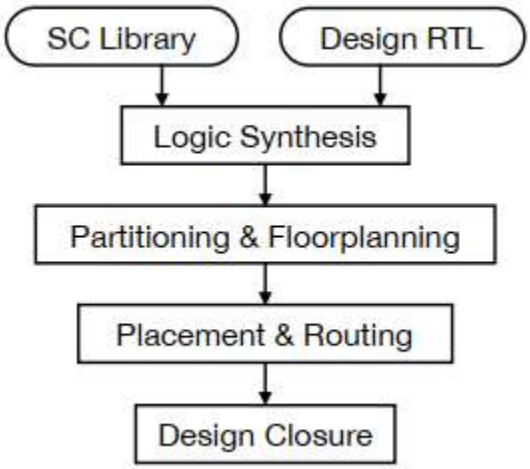
Moving towards the second study i.e. **"Design of a Custom Standard-Cell Library in 28nm CMOS".** This study compares the results of different standard cells on varying the parameters such as transistor sizing, threshold voltage, dimensions of power tracks, number of tracks in a standard cell and PVT corners. The conclusions on the basis of delay optimizations, leakage power consumption and delay has been made. The significance of clock tree synthesis over performance of the design is also been explained and verified with the results.The ultimate goal of the project is to analyze the design to cater the designing and fabrication of the 32-byte SPI .

The another study which is involved to lead to the proposed work is, **"Standard Cell Library Based Layout Characterization and Power Analysis for 10nm Gate-All-Around (GAA) Transistors".** The superior gate electrostatic control of the channel over FinFET, gate-all-around (GAA) transistor technology is one of the most promising candidates for ultimately scaled FETs. The parameters considered for analysis are ND, Ns, Nc, electrostatic-charge and threshold voltage.

As moved towards FinFET and GAA, one of the challenges is the discrete size of the fin and nanowire. Transistor width, which is one of the main variables for tweaking transistor sizes, is no longer a continuum. The driving strength of GAA transistor depends on geometrical parameters of nanowires. Thus, the GAA standard cell sizing involves selecting the appropriate number of nanowires for pull-up and pull-down networks of each logic cell. Here, in this study, a general sizing method is adopted that targets at balancing the rise and fall delays of a standard cell.

The next that we are referring to is, **"Standard Cell Library Design and Optimization Methodology for ASAP7 PDK".** This study mainly suggests two techniques for design and optimization of SC library namely Exhaustive transistor sizing and transistor placement with euler paths. In exhaustive transistor sizing, for a set of basic logic SCs, we obtain a set of most balanced pull-up and pull-down networks.Euler path theory generates optimal source/drain sharing for compact SC area.There may exist multiple area-

optimal Euler paths for a Standard cell library.The path with better pin accessibility and smaller pin capacitance is favoured. Further library-level optimizations are performed based on final PPA metrics from entire synthesis flow.



This is the synthesis flow of the study. This study revolves around the optimizations that can be took care of at 7nm technology node.

IV. CHARACTERIZATION METHOD

The idea is to focus on the library characterization of the combinational circuits (Inverter, NAND, NOR, MUX) and sequential circuits (D-FlipFlop, Adder) at three technology nodes i.e., 180nm, 90nm, 45nm. Library Characterization till date is done at any one technology node, mainly focusing on combinational circuits but the current work will be providing wide range of analysis of each cell (combinational and sequential) at three technology nodes at the same tool. It will cover analysis of all the cells on the basis of timing, power dissipation, area, threshold voltage and leakage current from higher to lower technology nodes. Addition to that analysis and results of PVT checks and TT corner of the cells at three technology nodes will also be captured. Schematic Simulations performed will mainly be transient in nature since the main focus is digital logic standard cells. The main purpose is to build understanding of the library characterization of the standard cells. This will also make it easy to understand the logical and physical functioning of the combinational and sequential logic gate with respect to time, area, power dissipation and leakage. All the cells will be framed using CMOS (Complementary Metal Oxide Semiconductor) technology and pass transistor technology.

V. CONCLUSION

The study till now has been made on either any of the cell or a technology node. The conclusion is to perform analysis on 12 cells i.e., Invereter, NAND, NOR, MUX, D-flipflop and full adder using CMOS and pass transistor technology at the three technology nodes(180nm, 90nm & 45nm). Addition to that the cells will be analyzed at 2 driving strengths (Nf=1,2). The standard cells then will be characterized on the basis of delay, leakage power and area at all design styles, driving strengths and design technology nodes. This will ultimately provide a large sum of data analysis points for academia and research purposes.

VI. FUTURE SCOPE

The future scope could be automation of the standard cell design using cadence language SKILL in collaboration with TCL (Scripting Language) in RedHat (Operating System) environment on the basis of given specifications. Developing a script to facilitate automated standard cell design generation.

VII. REFERENCES

[1] Xiaoqing Xu, Nishi Shah, Andrew Evans, Saurabh Sinha, Brian Cline1, and Greg Yeric 1ARM Inc., Austin, TX, USA, IEEE, INSPEC Accession Number: 17430566, ISSN: 1558-2434, ISBN: 978-1-5386-3094-5, 14th December 2017, "Standard Cell Library Design and Optimization Methodology for ASAP7 PDK"

[2] Jan Pliva, Rui Ma, Bastian Lindner, Laszlo Szilagyi, Florian Protze, Ronny Henker and Frank Ellinger Chair for Circuit Design and Network Theory Technische Universitat Dresden, 01069 Dresden, Germany, IEEE, INSPEC Accession Number: 16963905, ISBN: 978-1-5090-5582-1, 15th June 2017, "Design of a Custom Standard-Cell Library for Mixed-Signal Applications in 28 nm CMOS"

[3] Luhao Wang, Tiansong Cui, Shahin Nazarian, Yanzhi Wang and Massoud Pedram Department of Electrical Engineering University of Southern California, Los Angeles, CA, INSPEC Accession Number: 16836330, Electronic ISBN: 978-1-5090-1367-8, Electronic ISSN: 2164-1706, 24th April 2017, "Standard Cell Library Based Layout Characterization and Power Analysis for 10nm Gate-All-Around (GAA) Transistors"

[4] Mehmet A. Cirit Adaptec Inc. 691 South Milpitas Blvd. Milpitas, C A 95035, IEEE, INSPEC Accession Number: 4188640, ISBN: 0-7803-0015-7, 6th August 2002, "Characterizing a VLSI Standard Cell Library"

[5]Yu Yuan, Cecilia Garcia Martin and Erdal Oruklu Electrical and Computer Engineering Illinois Institute of Technology Chicago, IL, 60616,IEEE, INSPEC Accession Number: 15519747, 8th October 2015, "Standard Cell Library Characterization for FinFET Transistors using BSIM-CMG Models"

[6] Srujan R, Vinay S, Sruja m & Vishal M S, "Design, Implementation and Characterization of 45nm standard cell library for industrial synthesis flow", International Journal for Scientific Research & Development, ISSN: 2278-0181, NCESC – 2018 conference proceedings, Special issue – 2018