Virtual Paint Through Gesture Detection And Color Segmentation Technique Using DE2 FPGA Board

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Abstract

Object recognition and tracking with real-time camera assumes a significant job in numerous advanced vision applications, for example, work power following, insight observation, fire identification and some more. This research will be available a FPGA-based advanced control for a Virtual Paint. Virtual Paint venture use DE2board, 5 megapixel camera and a VGA Monitor, which is utilizes the camera to catch hand developments, so you can submit the air painting and showed on a LCD show, the entire procedure without utilizing mouse or joystick like gadget. The primary inspiration of this undertaking is to extricate the signal identification and shading division method from CMOS camera sensor to perform virtual paint. The control calculation will utilize a verilog language dependent on the utilization of sensible state graph.

Keywords— *Virtual painting board, Gesture detection, color segmentation, FPGA & Embedded System*

I. INTRODUCTION

Virtual paint is a system which can be used to draw colored pictures on any plain surfaces like a wall using hand movements and fingers with colored bands. This project draws its motivation from the sixth sense where using different gesture detection and color segmentation techniques while a software running on a handheld computing device performs a variety of different tasks like making notes in the air, reading a newspaperwith projected videos, capturing photographs using hand actions and even painting on walls. Intrigued by the scope of the project, we decided to do something similar in hardware. So, within the constraints of availability of hardware and time we implemented Virtual Paint.

II. LITERATURE REVIEW

M. Petouris, A. Kalantzopoulos and E. Zigouris [1] entitled "A Fpga-Based Digital Camera System Controlled from a LCD Touch Panel" proposed presents the plan and execution of such an open FPGA dependent on Digital Camera System for picture catching and continuous picture handling. Pictures caught with a CMOS sensor are at first put away in the framework's memory and afterward they are shown on a LCD Touch Panel. The principle objective of this proposed design is to be utilized as a stage to actualize and test propelled picture handling calculations. Separated of this, the framework underpins the control of the picture sensor, through the LCD Touch Panel. Furthermore, can speak with a PC through a JTAG interface for putting away the pictures on it. The proposed FPGA-based Digital Camera System, because of the FPGA adaptability, is for the most part focused to be utilized as an open and minimal effort stage for executing and testing ongoing picture preparing calculations. What's more the misuse of LCD Touch Panel can successfully aid the control of more cameras' parameters. Picture preparing calculations can happen previously or after the information putting away and due to the FPGA' s nearness, framework can be effectively altered. Tentative arrangements are to implant and test progressively advance picture preparing calculations because of the way that there is sufficient space left in the FPGA. What's more, we plan to make an all-inclusive menu for the LCD contact board. Growing such a menu the client can completely and in a well disposed way control camera's usefulness. Through this menu the client can likewise effectively select the execution of the attractive picture handling calculation.

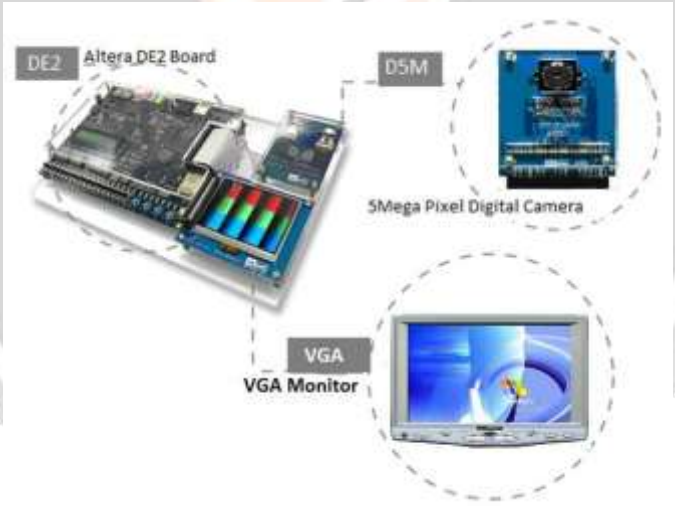
In the mean time, Suh Ho Lee, Seon Wook Kim, and Suki Kim [2] entitled "Execution of a Low Power Motion Detection Camera Processor Using a Cmos Image Sensor" proposed presents a low power movement identification camera processor, called Bluebox. It incorporates an ARM inserted microchip and a few designed modules utilizing pseudo Advanced Microprocessor Bus Architecture (AMBA). For decreasing force utilization, we utilize straightforward, however productive programming and

equipment strategies. We propose another movement location calculation to utilize just one piece for each pixel without loss of precision, and in this way it needs little figuring force and fulfills ongoing preparing prerequisites. What's more, we plan a power the board plan to control framework tickers for power decrease. Our proposed engineering is executed and confirmed in a FPGA with a CIS (CMOS Image Sensor).

Moreover, Mohamed Nasir Bin Mohamed Shukor, Lo Hai Hiung and Patrick Sebastian [3] entitled "Usage of Color Filtering on Fpga" proposed presents the development of a constant equipment picture handling framework on Field Programmable Gate Array (FPGA). The picked picture preparing calculation is a solitary shading Filtering calculation. This work uses Altera DE2 improvement board engaged by the Cyclone II FPGA combined with a 5 Mega pixel CMOS camera from Terasic Technologies. Verilog HDL is picked as the equipment programming language for this framework and its gathered utilizing Quartus II program. The usefulness of the calculation is first confirmed in Matlab, mimicking the normal yield of the framework before executing it onto the FPGA improvement board. shading Filtering calculations are effectively executed on Cyclone II FPGA.
In conclusion, Nai-Jian Wang, Sheng-Chieh Chang and Pei-Jung Chou [4] entitled "A Real-Time Multi-Face Detection System Implemented On FPGA" proposed a continuous multi-face identification framework dependent on equipment configuration to improve the handling time. The proposed equipment engineering is actualized on Altera DE2-70 improvement board to test the practicality of our equipment structure. The execution of our framework requires 15,223 rationale components. It can work progressively at an edge rate of 30fps, and identify up to five faces at the same time. The test result demonstrates that our proposed face location design accomplishes a continuous dependable framework with minimal effort and high identification rate.

III. PROPOSED SYSTEM

The product put in the FPGA is actualized in Verilog. It gives module level recreation and confirmation, which is permits developing the structure from littler modules. When the reproduction, union and time check is confirmed in the Quartus programming, at that point the software engineer gadget apparatus will stack the bit document of Verilog onto the FPGA utilizing the USB blaster.

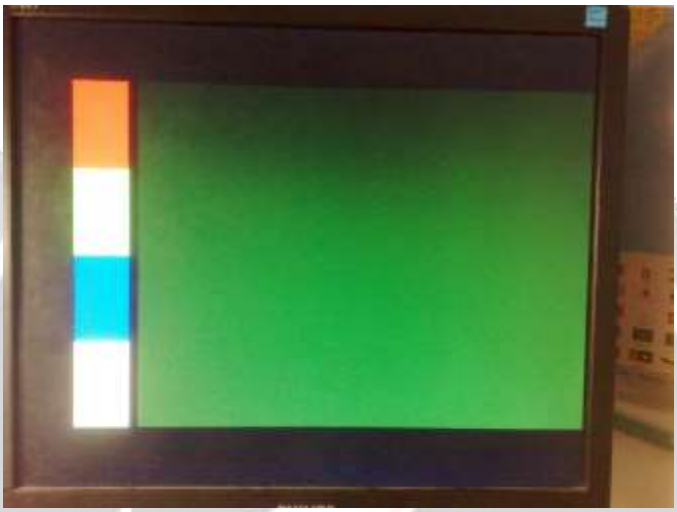


A module for illustration lines, we have for the location of the middle pixel shading space draw lines, yet in addition for smoothing the progressive picture outlines in the two pixels between the determined focus pixel. For essential activity area, the most significant is to acknowledge how to distinguish the red, yellow and green. By contrasting the RGB esteems and the limit esteem, and ascertains the sweep and the RGB estimations of every pixel to accomplish relationship. After discovery of a particular shading, as per the identified shade of the predetermined esteem is put away in memory. Some portion of the choice by a line drawing put away location.
For M4K perusing part is consistently perused qualities and sent to the VGA. Yellow for painting and select the shading, red is utilized to control pen up and pen down task, so when the red is recognized penup mode is activated, quit drawing. So as to take out commotion on the screen, we determine previously and now put away in the pixel memory 20 ought to have a length addresses. M4K information put away qualities are two shading decisions. It demonstrates to us what is the shading utilized for illustration which one, you can utilize the shading determination. In outline, we utilize four shades of the illustration with white eradicated. The eraser size of 3 × 3 pixels square. Our red recognition incentive to control whether the illustration. M4K memory in each incentive in

the location comparing to the VGA show pixel address. When we read M4K, we as per the information read from the memory to yield explicit RGB shading esteems. 01 yield red, 10 green, 11 blue, 00 white. VGA_controller module peruses these qualities and yield them on the screen. The screen yield shading bar by moving the cursor to the assigned region, select the shading throughput pen to paper, pen is red. As in the mouse, snap and discharge.

IV. RESULTS

The task has been made dependent on Verilog language which is run utilizing the Quartus 11.1 programming. Gathered data gave on the site and research paper about strategies and programming activity is painstakingly broke down. In light of gathering data, the fundamental test is to set up cursor development that not reaction to the predetermined target shading.



IV. CONCLUSION

The structure and usage of a virtual painting board in an FPGA board. The framework has a CMOS camera as an information gadget and a VGA screen as a yield gadget. Userscan draw lines, shading an image or both and can tail it on the VGA screen. The workis developed based on VHDL and Verilog HDLwhich arerun utilizing the Quartus11.1 software.The framework equipment consists of CCD_capture, RAW2RGB, SDRAM, Main Ctrl, M4K, and VGA controller. The framework identifies a yellow and redcolour with the camera and stores and changes over the organize. In view of Altera DE2 board, we utilize 5M pixel CMOS camera, VGA monitor,and shaded band for this framework. It will be considerably more commonsense on the off chance that it is perceived distinctly by the development of the hands without shading groups utilized in this work.Also, it requires text style modification and different shading underpins.

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